REMARKS

In the above-identified Office Action, the Examiner has objected to the drawings because the block circuits shown in Figures 1 and 5 do not have text labels. Applicant assumes that the Examiner is referring to the block circuits in Figures 1 and 4 and hereby submits corrected drawings labeling such block circuits.

The Examiner has objected to the Abstract, as well as the Title. Applicant by the above amendments have submitted a new Abstract and a new Title, and as such, these objections are considered obviated.

Claim 5 has been objected to because of certain noted informalities. Applicant has amended claim 5 so that it should obviate these objections.

Claims 5-6 have been rejected as being indefinite. The Examiner has stated that claim 5 fails to particularly point out the structurally relationships between the elements. This and other matters raised because of indefiniteness have been corrected.

Claims 5 and 6 have been rejected as being anticipated by the patent to McCollum et al. Applicant has amended claims 5 and 6, and as amended, believes such claims recite over McCollum et al. More specifically, McCollum et al., United States Patent No. 6,028,460, is different to the subject matter of present claim 1 in two basic ways.

The loop of the digital phase detector contains an information of the phasing; thus, if the analog loop of the analog phase detector is connected together with the digital phase detector, the phasing between the reference and the voltage controlled oscillator (VCO) is not arbitrary, since the digital filter also contains information of the phase difference between the reference and the VCO. According to the present invention, only a quantisation error remains on the output of the analog phase detector. This quantisation error amounts to a maximum of one clock of the VCO. By activating the analog phase detector, this phase error is reduced until the phase error is zero.

In contrast to this, McCollum et al. discloses a PLL-circuit which is well-known and has been made for a couple of decades in so-called clock and data recoveries. Particularly with regard to PLL-circuits, the digital PLL loop in McCollum et al. serves as a frequency acquisition. This digital loop, however, contains no information about the phasing. Thus, in McCollum et al., if the

PLL-circuit is switched to the analog loop, the phasing between the reference and the VCO is arbitrary.

As a result of the above differences, McCollum et al. is not an analogus structure to that of the subject invention. According to the present invention, the electronic phase locked loop (PLL-circuit) contains a digital filter having a consequential quantisation error. In contrast to this, McCollum et al. discloses an analog filter and a switching between a frequency detection and phase detection. The PLL-circuit according to McCollum et al. can not perform a frequency detection, and a phase detection at the same time.

Another difference between the present invention and the disclosure of McCollum et al. lies in the switching. In McCollum et al., a switching means (500) is disclosed which is used to switch between the digital PLL loop (300) and the analog PLL loop (200). That means, in McCollum et al., either the digital PLL or the analog PLL is activated, but not both PLL loops.

According to the present invention, the digital PLL loop is always activated. The analog PLL loop may be activated and connected in parallel to the digital loop. In this operation mode, the digital PLL loop and the analog PLL loop operate together. Therefore, the operation modes are also different in McCollum et al. when compared with the present invention.

Applicants hereby request reconsideration and reexamination thereof.

With the above amendments and remarks, this application is considered ready for allowance and Applicants earnestly solicit an early notice of same. Should the Examiner be of the opinion that a telephone conference would expedite prosecution of the subject application, he is respectfully requested to call the undersigned at the below-listed number.

Respectfully submitted,
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ABSTRACT

The subject invention comprises an electronic phase-locked loop of digital design, supplemented by an additional analog phase detector (APD), which enables the phase error ("jitter") to be attenuated. The phase-locked loop may be used as an integrated circuit in integrated services communications networks, data communication or networks.